REMARKS

Reconsideration and allowance of the above-referenced application are respectfully requested.

Upon entry of the amendment, claims 1-17 will remain in the application.

Claims 1 and 2 were rejected under 35 U.S.C. 103(a) as being allegedly unpatentable over Wada et al. (US 6,225,846, hereinafter "Wada"), in view of Fujita et al. (US 6,215,159, hereinafter "Fujita").

Claims 3-17 were rejected under 35 U.S.C. 103(a) as being allegedly unpatentable over Wada in view of Fujita and further in view of Rossi et al. (US 6,069,513, hereinafter "Rossi").

Claims 11-17 were rejected under 35 U.S.C. 103(a) as being allegedly unpatentable over Wada and Fujita in view of Rossi and further in view of Gillingham et al. (US 6,510,503, hereinafter "Gillingham").

Applicants respectfully traverse these rejections.

Applicants teach a dynamic bus repeater circuit with an improved noise margin of Vcc/2. This noise margin is closer to that of a static bus repeater than standard dynamic repeaters which may have a noise margin only slightly higher than the threshold voltage (V_T) of the input transistor. The bus repeater is a dynamic circuit, i.e., it is clocked and has a pre-charge stage in which the value on the input node does not affect the output, and an evaluation stage in which the value on the input does affect the output.

The examiner states in the Response to Arguments section that Fujita discloses in figures 6A-6B that the input signal of a certain voltage could give the same voltage at the output, indicating in the Advisory Action mailed December 26, 2002 that

this would satisfy Applicants' definition of "noise margin" as defined in the Specification at page 6, paragraph [0015].

The invention deals with switching circuits, and "noise margin" refers to the voltage at which the circuit will switch, not merely that an input signal of certain voltage could give same voltage at the output. Consider page 7, paragraph [0018], which states:

"The feedback inverter 310 provides an additional delay to switching in response to a noise signal. When a noise signal exceeds Vcc/2, the input NMOS transistor 324 starts to turn on, opening a path to Vss, and starts to turn off the lower pull-up PMOS transistor 306, closing the path to Vcc. … Thus, the noise signal must exceed Vcc/2 for a sufficient amount of time to cause the output node to switch to a HIGH state." (emphasis added).

"Noise margin" refers to the voltage the input must exceed to cause the circuit to switch. In this case, the noise margin is Vcc/2, which equates to half of the difference between the logical HIGH (Vcc) and the logical LOW (Vss) signals (see paragraph [0016] on pages 6 to 7 for definitions of source voltage Vcc and sink voltage Vss as logical HIGH and LOW, respectively). This is much higher than the noise margin of other dynamic circuits, which tend to be close to the threshold voltage of the input transistor.

Fujita does not show a circuit with a noise margin of Vcc/2. Rather, figures 6A and 6B merely show that a logical HIGH input signal (Vdd) will cause the circuit to switch all the way to a logical HIGH signal at the output. The input signal SIG only switches between logical LOW and logical HIGH values. The figures give no indication as to the value of the noise margin for this circuit.

Applicants are amenable to amending the claims to clarify this distinction, for example, substituting "$(V_{HIGH} - V_{LOW})/2$" or "$(V_{source} - V_{sink})/2$" for "Vcc/2" in the claims.

None of Wada, Fujita, Rossi, and Gillingham teaches or suggests, either alone or in combination, a dynamic bus repeater with a noise margin of Vcc/2. Accordingly, Applicants submit that independent claims 1 and 11 and their dependencies are allowable.